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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,561	12/21/2000	William R. Wheeler	10559-261001/P9032	7938

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EXAMINER	
SHAAWAT, MUSSA	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,561	WHEELER ET AL.	
	Examiner	Art Unit	
	Mussa A Shaawat	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to application number 09/745,561. Claims 1-18 are presented for examination.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "application 1 through N" in Paragraph [0020], "processors 1 through N" Paragraph [0020], and reference # "30" in Paragraph [0025]. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

Abstract is more than 150 words, appropriate action is required. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "the," should be avoided. The

abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Geoffrey J. Bunza US Patent No. (5,838,948) referred to hereinafter as Bunza.

3. As per claim 1, Bunza teaches a method comprising: providing a first processor (col.2 lines 52-53) on a single silicon chip (see Fig.5 block # 100); loading, on the first processor, a software simulation (col.2 lines 54-55, storing a set of instructions in memory of a processor to be executed is inherently loading a set of instructions to memory) of a second processor (col.2 lines 52-53) that is to be provided in hardware on the single silicon chip (see Fig. 5 block 100, the hardware of the microprocessors is shown); loading, on the first processor (col.2 lines 52-53), an applications software (see col.6 lines 1-10, compiling a target program into an object code and then downloading it to a processor memory) that is to be executed on the hardware of the second processor (col.2 lines 52-53, see hardware simulator, Fig. 1 block 20); and executing the

software simulation (see col.2 lines 55-61, processor emulator receives the computer instructions from memory, which serves as a software simulation) of the second processor (col.2 lines 52-53) and the applications software on the first processor (see col.2 lines 52-55, executing computer instruction is similar to executing an application software).

4. As per claim 2, Bunza teaches a method of claim 1: wherein the software simulation of the second processor (col.2 lines 52-53) includes a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor; and further comprising selecting the software simulation as either the slow, highly detailed simulation or the fast, high-level simulation, (see col.11 lines 47-67, high speed processor emulator, and a slow software simulator, which correspond to the fast and slow detailed simulation).

5. As per claim 3, Bunza teaches a method of claim 2 wherein the slow, highly detailed simulation of the second processor (col.2 lines 52-53) includes a simulation of bus interface to the second processor and to memory and control status registers (see col.10 lines 20-35, hardware simulator simulates the interactions between the target microprocessor = corresponds to second processor, and target circuitry, including a data base interface).

6. As per claim 4, Bunza teaches a method of claim 1 wherein: loading, on the first processor (col.2 lines 52-53), a simulation (col.2 lines 54-55, storing a set of instructions in memory of a processor to be executed is inherently loading a set of instructions to memory) of a second processor (col.2 lines 52-53) that is to be provided in hardware on the single silicon chip (see Fig. 5 block 100, the hardware of the microprocessors is shown) includes loading, on the first processor, a plurality of software simulations of a plurality of second processors that are to be provided in hardware on the single silicon chip, each software simulation corresponding to

one of the second processors, (see col.2 lines 52-55, executing computer instruction is similar to executing an application software).

7. As per claim 5, Bunza teaches a method of claim 4 wherein: said loading, on the first processor (col.2 lines 52-53), an applications software that is to be executed on the hardware of the second processor (col.2 lines 52-53) includes loading (see col.6 lines 1-10, compiling a target program into an object code and then downloading it to a processor memory), on the first processor, a plurality of applications software, each applications software to be executed on the hardware of a corresponding one of the plurality of second processors (see col.1 lines 62-67, col.2 lines 1-7, processor emulator emulates a plurality of software instruction or applications).

8. As per claim 6, Bunza teaches a method of claim 5 wherein: said executing the software simulation of the second processor (col.2 lines 52-53) and the applications software on the first processor (see col.2 lines 52-55, executing computer instruction is similar to executing an application software) includes executing the plurality of software simulations of the plurality of second processors and the plurality of applications software on the first processor (see col.2 lines 14-17, et seq., simulation processor simulating a plurality of computer instructions).

9. As per claim 7, Bunza teaches a method wherein each software simulation of the second processor (col.2 lines 52-53) includes a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor; and further comprising selecting each software simulation as either the slow, highly detailed simulation or the fast, high-level simulation, (see col.11 lines 47-67, high speed processor emulator, and a slow software simulator, which correspond to the fast and slow detailed simulation).

10. As per claim 8, Bunza teaches a method of claim 1 further comprising: providing a third processor external to the single silicon chip, (see col.3 lines 60-67, external to the chip is an IC circuit or ASIC which corresponds to the third processor communicating with the microprocessor which corresponds to second processor inside the chip); wherein the software simulation of the second processor includes a first interface (see col.2 lines 1-8); configuring the first interface to execute the software simulation of the second processor on the third processor (see col.3 lines 65-67, the external IC circuit executes the software program); loading, on the third processor, the software simulation (col.2 lines 54-55, storing a set of instructions in memory of a processor to be executed is inherently loading a set of instructions to memory) of the second processor (col.2 lines 52-53); wherein the applications software includes a second interface (see col.2 lines 23-30, et seq.); configuring the second interface to execute the applications software on the third processor; loading, on the third processor, the applications software; and executing the software simulation of the second processor and the applications software on the third processor (see col.6 lines 1-13, the code is compiled and downloaded into memory of processor).

11. As per claim 9, Bunza teaches a method of claim 1 further comprising: providing the second processor (col.2 lines 52-53) as hardware on the single silicon chip (see Fig. 5 block 100, the hardware of the microprocessors is shown); wherein the applications software includes an interface (see col.2 lines 1-8); configuring the interface to execute the applications software on the hardware of the second processor (see col.3 lines 65-67, the external IC circuit executes the software program); and executing the applications software on the hardware of the second processor (see col.6 lines 1-13, the code is compiled and downloaded into memory of processor).

12. As to claim 10, Bunza teaches a computer program product embodied on a tangible storage medium, the program comprising executable instructions that enable the computer to: configure a software simulation of a first processor (col.2 lines 54-55, storing a set of instructions in memory of a processor to be executed is inherently configuring a set of instructions to memory), which is to be provided in hardware on a single silicon chip (see Fig.5 block # 100), to execute on a second processor on the single silicon chip in either a slow, highly detailed simulation mode or a fast, high-level simulation mode (see col.11 lines 47-67, high speed processor emulator, and a slow software simulator, which correspond to the fast and slow detailed simulation); and configure a first applications software, which is to be executed on the hardware of the first processor (see col.2 lines 55-61, processor emulator receives the computer instructions from memory, which serves as a software simulation), to execute with the software simulation of the first processor on the second processor or to execute on the hardware of the first processor (see col.2 lines 52-55, executing computer instruction is similar to executing an application software).

13. As per claim 11, Bunza teaches a computer program product embodied on a tangible storage medium of claim 10, the program further comprising executable instructions that enable the computer to: configure a second applications software to execute on either the second processor or a processor external to the single silicon chip (see col.6 lines 1-10, compiling a target program into an object code and then downloading it to a processor memory).

14. As per claim 12, Bunza teaches a method of developing software for a multi-processor chip, the method comprising: loading, on a first processor, a plurality of software simulations (col.2 lines 54-55, storing a set of instructions in memory of a processor to be executed is

inherently loading a set of instructions to memory) of a plurality of second processors that are to be provided in hardware on a single silicon chip (see Fig.5 block # 100), each software simulation corresponding to a one of the second processors, and each software simulation includes a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor ; selecting each software simulation as either the slow, highly detailed simulation or the fast, high-level simulation (see col.11 lines 47-67, high speed processor emulator, and a slow software simulator, which correspond to the fast and slow detailed simulation); loading, on the first processor, a plurality of applications software (col.2 lines 52-53) includes loading (see col.6 lines 1-10, compiling a target program into an object code and then downloading it to a processor memory), each applications software to be executed on the hardware of a corresponding one of the plurality of second processors (see col.1 lines 62-67, col.2 lines 1-7, processor emulator emulates a plurality of software instruction or applications); and executing the plurality of software simulations of the plurality of second processors (see col.2 lines 52-55, executing computer instruction is similar to executing an application software) and the plurality of applications software on the first processor (see col.2 lines 14-17, et seq., simulation processor simulating a plurality of computer instructions).

15. As per claim 13, Bunza teaches a method of claim 12 wherein the slow, highly detailed simulation of the second processor includes a simulation of bus interface to the first processor and to memory and control status registers (see col.10 lines 20-35, hardware simulator simulates the interactions between the target microprocessor = corresponds to second processor, and target circuitry, including a data base interface).

16. As per claim 14, Bunza teaches a method of claim 12 further comprising providing the first processor as hardware on the single silicon chip, (see Fig. 5 block 100, the hardware of the microprocessors is shown).

17. As per claim 15, Bunza teaches a method of claim 12 further comprising providing the first processor as hardware external to the single silicon chip, (see col.3 lines 60-67, external to the chip is an IC circuit or ASIC communicating with the microprocessor inside the chip).

18. As per claim 16, Bunza teaches a method of claim 12 further comprising: providing a one of the plurality of second processors as hardware on the single silicon chip, (see Fig. 5 block 100, the hardware of the microprocessors is shown); wherein each of the plurality of applications software includes an interface, (see col.2 lines 1-8); configuring the interface of the applications software corresponding to the one of the plurality of the second processors to execute the applications software corresponding to the one of the plurality of the second processors on the hardware of the one of the plurality of second processors; and executing the applications software on the hardware of the second processor, (see col.2 lines 52-55, executing computer instruction is similar to executing an application software).

19. As per claim 17, Bunza teaches an apparatus for developing software for a multi-processor chip comprising: a first processor on a single silicon chip (see Fig.5 block # 100) having loaded thereon, a software simulation (col.2 lines 54-55, storing a set of instructions in memory of a processor to be executed is inherently loading a set of instructions to memory) of a second processor that is to be provided in hardware on the single silicon chip (see Fig.5 block # 100), and an applications software that is to be executed on the hardware of the second processor (see col.2 lines 52-55, executing computer instruction is similar to executing an application

software); the first processor to execute the software simulation of the second processor and the applications software on the first processor (see col.2 lines 55-61, processor emulator receives the computer instructions from memory, which serves as a software simulation).

20. As per claim 18, Bunza teaches an apparatus of claim 17 further comprising: a third processor external to the single silicon chip having loaded thereon the software simulation of the second processor and the applications software, (see col.3 lines 60-67, external to the chip is an IC circuit or ASIC which corresponds to the third processor communicating with the microprocessor which corresponds to second processor inside the chip); the third processor to execute the software simulation of the second processor and the applications software, (see col.3 lines 65-67, the external IC circuit executes the software program).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Bonola US Patent No. (5,953,516) Method and apparatus for emulating a peripheral device to allow device driver development before availability of the peripheral device.
- Sniderman et al. US Patent No. (6,028,996) method and apparatus for virtualizing system operation.
- Pauna US Patent N. (6,052,524) system and method for simulation of integrated hardware and software components.
- Bunza et al. US Patent No. (6,571,373) Simulator-independent system on chip verification methodology.

- Devins et al. US Patent No. (6,427,224) Method for efficient verification of system-on-chip integrated circuit designs including an embedded processor.
- Bonola US Patent No. (6,321,279) system for implementing intelligent I/O processing in a multi-processor system.
- Willis et al. (5,999,734) compiler-oriented apparatus for parallel compilation, simulation and execution of computer programs and hardware models.
- Rajsuman et al. US patent No. (6,678,645) method and apparatus for soc design validation.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (703) 605-1372. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (703) 308-6647. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Examiner

September 20, 2004

JEAN B. HOMERE
PRIMARY EXAMINER